PCMCIA Linear Flash Memory Card

CardPro™ International

Linear Flash Intel/Sharp S5 Memory Card *2MB, 4MB, 8MB, 16MB*

General Description

CardPro™*2000* Intel/sharp S5 Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

CardPro™*2000* Intel/Sharp S5 Flash cards conform to PCMCIA international standard.

The card's control logic provides the system interface and controls the internal Flash memories. Card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), **CardPro™*2000*** Intel/Sharp S5 Flash cards provide removable high-performance disk emulation.

CardPro™*2000* Intel/Sharp S5 Flash cards offers low power modes controlled by registers. Standard cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

CardPro™*2000* Intel/Sharp S5 is based on Intel/Sharp 28F016S5 Flash memories.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

Features

- Low cost High Density Linear Flash Card
- Supports 5V only systems
- Based on Intel/Sharp FlashFile Devices
- Fast Read Performance
  - 90ns Access Time
- x8 / x16 Data Interface
- High Performance Random Writes
  - 8µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Architecture Overview

CardPro™*2000* Intel/Sharp S5 is designed to support from qty 2 to 8 of 16Mb devices, providing a range of density options. Cards are based on the 28F016S5 (16Mb) devices for 5V only applications. Devices code for the 28F016S5 is AAH. Cards utilizing the 16Mb components provide densities of 2MB, 4MB, 8MB, 16MB.

In support of the PC Card 95 standard for word wide access devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7.

CardPro™*2000* Intel/Sharp S5Flash cards supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register.

CardPro™*2000* Intel/Sharp S5 Flash cards conform with the PC Card Standard (PCMCIA) and JEIDA 4.2, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

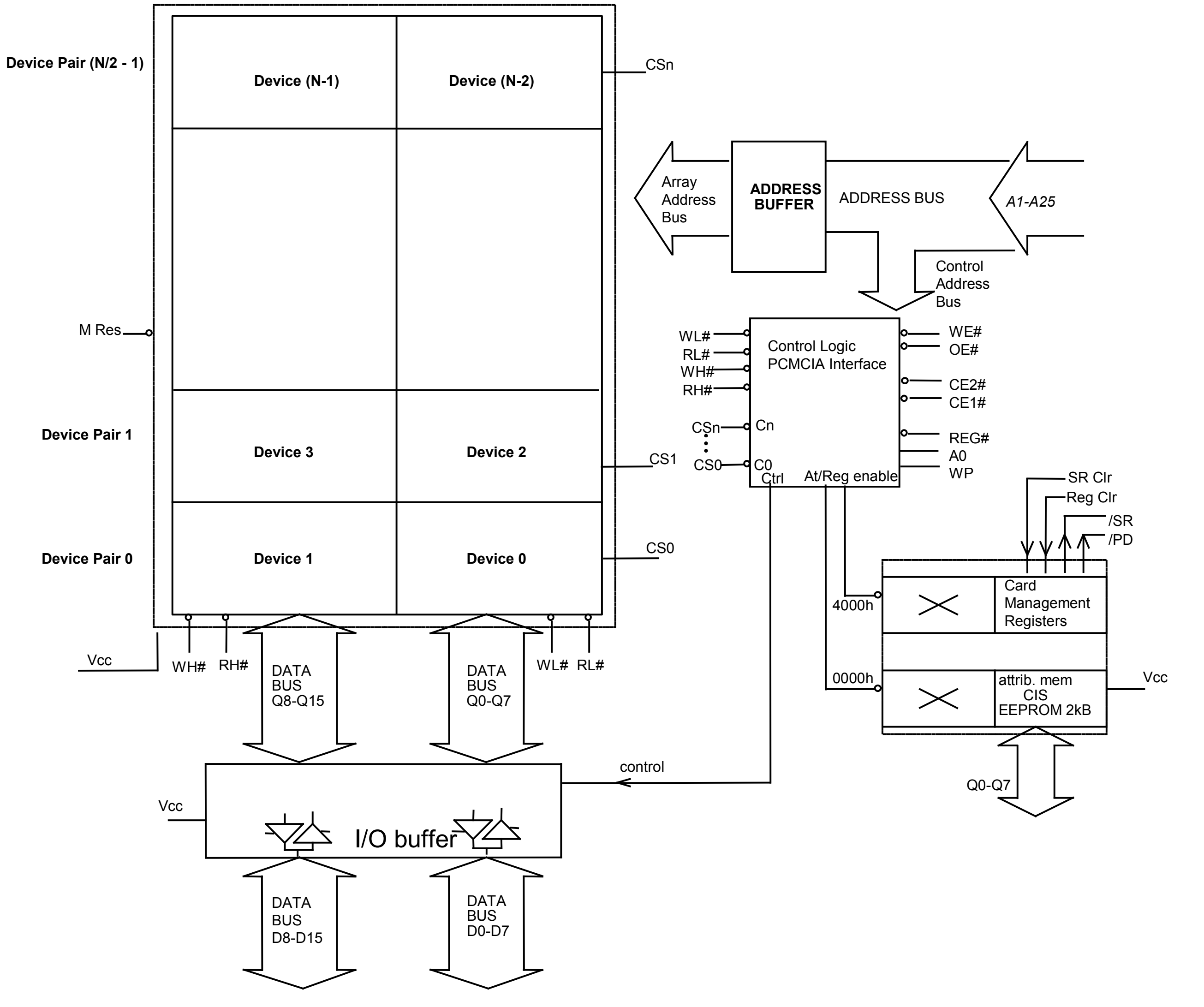
Standard cards are shipped with **CardPro™ *2000*** Linear Flash Logo. Cards are also available with custom labeling using only primary colours and simple artwork.

PCMCIA Linear Flash Memory Card

CardPro™ International

Block Diagram

Device type	Manuf ID	Device ID
28F016S5	89_H	AA_H



Registers in Attribute Memory Space

ADDRESS	Register NAME
4100h	Status Reg.
4002h	Config. and Status Reg.
4000h	Configuration Option Register

COR

Configuration Option Register: ADRS=4000h Write Only

SRES	LREQ	-Configuration Index-					
D7	*D6*	D5	D4	D3	D2	D1	D0

D7 Soft Reset, active High
1 = Reset State
0 = End Reset State
D6 LevelReq (not supported)
D5-D0 Configuration index (not supported)

CSR

Configuration Status Register: ADRS=4002h Write Only

not supported					PDwn	not supported	
D7	*D6*	*D5*	*D4*	*D3*	**D2**	*D1*	*D0*

D2 Power Down; active High
1=Place all memory devices in power down mode
0=normal operation Power On default=0

SR

Status Register: ADRS=4100h Read Only

not supported		SReset		PDwn	not supported		R/BSY
D7	*D6*	**D5**	D4	**D3**	*D2*	*D1*	**D0**

D5 Represents the state of SRESET bit in COR (4000h)
1=Reset
0=Normal operation
Power On default D5=0
D3 Represents the state of Power Down bit (D2) in CSR (4002h)
1=Power Down
D0 Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs.This bit allows software polling of the card's Ready/Busy status.
1=Ready

PCMCIA Linear Flash Memory Card

CardPro™ International

Pinout

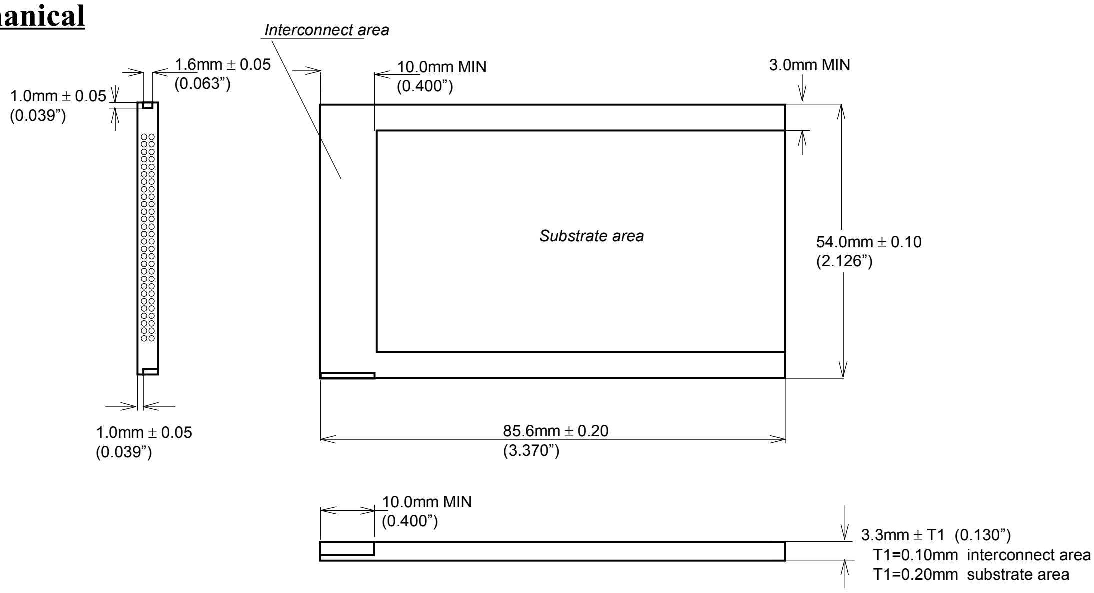
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY**#**	O	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	2MB(3)
50	A21	I	Address bit 21	4MB(3)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(3)
54	A23	I	Address bit 23	16MB(3)
55	A24	I	Address bit 24	N.C.
56	A25	I	Address bit 25	N.C.
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	Low(2)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(2)
63	BVD1	O	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

1.RDY/BSY signal is an “Open drain” type output.
2. Wait#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 4MB A21 is MSB, A22 - A25 are NC).

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A23 enable direct addressing of up to 16MB of memory on the card. Signal A0 is not used in word access mode. A23 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages for card (12V). Not connected for 5V only card.
VCC		**CARD POWER SUPPLY:** (5.0V).
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V card .
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Functional Truth Table

READ function						*Common Memory*			*Attribute Memory*		
Function Mode	/CE2	/CE1	A0	/OE	/WE	/REG	D15-D8	D7-D0	/REG	D15-D8	D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

Absolute Maximum Ratings [1]

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Storage Temperature	
Commercial	-30°C to +80 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Note:
(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics [1]

Symbol	Parameter	Density (Mbytes)	Notes	Typ[3]	Max	Units	Test Conditions
I_{CCR}	VCC Read Current	All			35	mA	VCC = VCCmax tcycle = 150ns,CMOS levels
I_{CCW}	VCC Program Current	All			75	mA	
I_{CCE}	VCC Erase Current	All			100	mA	
I_{CCS} (CMOS)	VCC Standby Current	2MB	2	60		µA	VCC = VCCmax
		4MB		60			Control Signals = VCC
		16MB		180			Reset = VSS, CMOS levels

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Byte wide operations. For 16 bit operation values are double.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	VCC = VCCMAX Vin =VCC or VSS
I_{LO}	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vout =VCC or VSS
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7VCC	VCC+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
V_{LKO}	VCC Erase/Program Lock Voltage	1	2.0		V	

Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when VIN=VCC due to internal pull-down resistor.

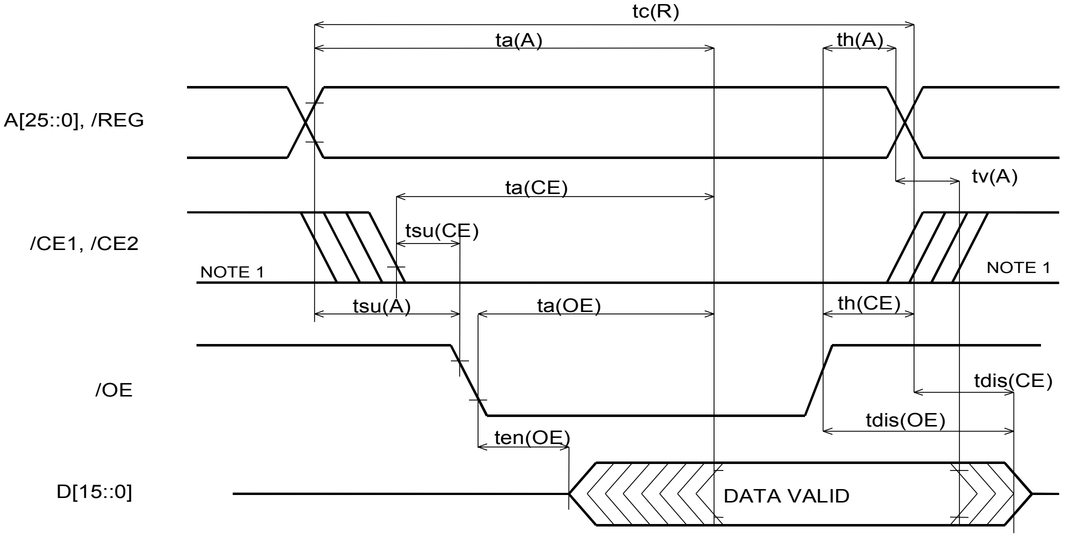
AC Characteristics

Read Timing Parameters

		90ns		
SYMBOL (PCMCIA)	Parameter	Min	Max	Unit
$t_c(R)$	Read Cycle Time	90		ns
$t_a(A)$	Address Access Time		90	ns
$t_a(CE)$	Card Enable Access Time		90	ns
$t_a(OE)$	Output Enable Access Time		75	ns
$t_{su}(A)$	Address Setup Time		20	ns
$t_{su}(CE)$	Card Enable Setup Time		0	ns
$t_h(A)$	Address Hold Time		20	ns
$t_h(CE)$	Card Enable Hold Time		20	ns
$t_v(A)$	Output Hold from Address Change		0	ns
$t_{dis}(CE)$	Output Disable Time from CE#		75	ns
$t_{dis}(OE)$	Output Disable Time from OE#		75	ns
$t_{en}(CE)$	Output Enable Time from CE#	5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		ns
$t_{rec}(RSR)$	Power Down recovery to Output Delay. VCC = 5V		500	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



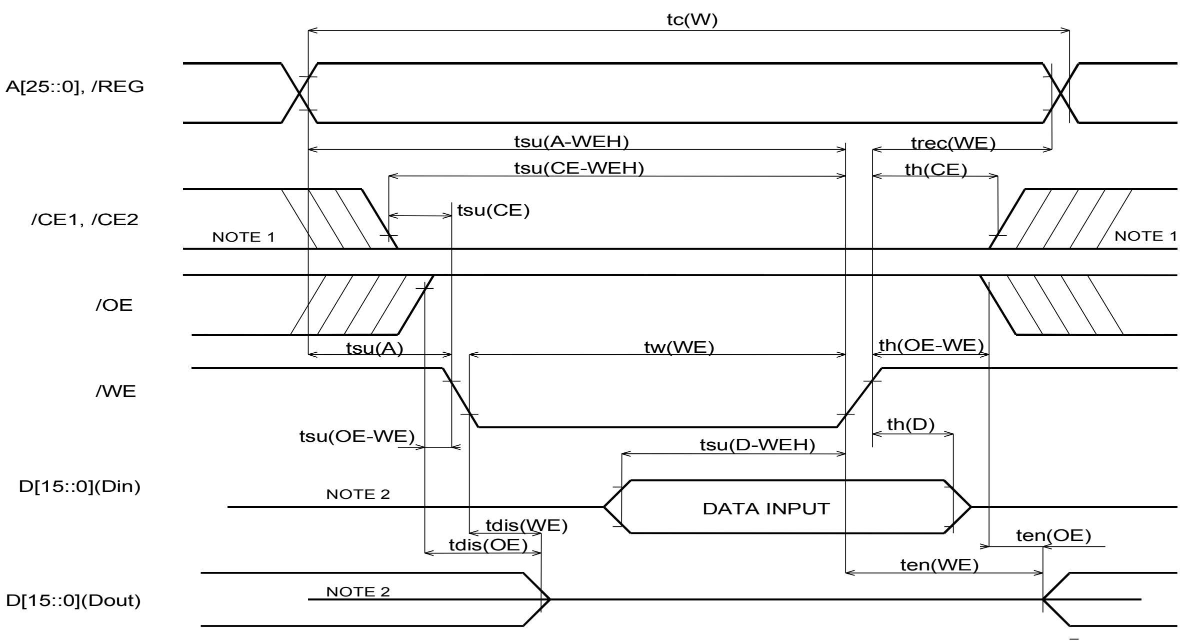
Note: Signal may be high or low in this area.

Write Timing Parameters

		90ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_cW	Write Cycle Time	90		ns
$t_w(WE)$	Write Pulse Width	80		ns
$t_{su}(A)$	Address Setup Time	20		ns
$t_{su}(A\text{-}WEH)$	Address Setup Time for WE#	100		ns
$t_{su}(CE\text{-}WEH)$	Card Enable Setup Time for WE#	100		ns
$t_{su}(D\text{-}WEH)$	Data Setup Time for WE#	50		ns
$t_h(D)$	Data Hold Time	20		ns
$t_{rec}(WE)$	Write Recover Time	20		ns
$t_{dis}(WE)$	Output Disable Time from WE#		75	ns
$t_{dis}(OE)$	Output Disable Time from OE#		75	ns
$t_{en}(WE)$	Output Enable Time from WE#	5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		ns
$t_{su}(OE\text{-}WE)$	Output Enable Setup from WE#	10		ns
$t_h(OE\text{-}WE)$	Output Enable Hold from WE#	10		ns
$t_{su}(CE)$	Card Enable Setup Time from OE#	0		ns
$t_h(CE)$	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance (1,3)

VCC = 5V ± 5%, T_A = 0C to + 70C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1}	Word/Byte Program time	4		8		µs
t_{EHQV2}	Block Program Time	device S5	0.4	0.5		sec
	Block Erase Time	device S5	0.9	1.1		sec

Notes:

1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

Card Family and Version Information

FL16-090-02M-11189S5	2 MBYTES
FL16-090-04M-11189S5	4 MBYTES
FL16-090-08M-11189S5	8 MBYTES
FL16-090-16M-11189S5	16 MBYTES

Similar range of FLASH Card using AMD memory devices also available from CardPro™ International

CardPro™ International
The Trading Arm of Card Professionals Ltd
6 Constable Way, Sandhurst, Berkshire, GU47 0FE United Kingdom
Registered Offices as above

Tel: +44(0)1276 609777

Email: sales@cardprointernational.com Web: www.cardprointernational.com